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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,225	FORBES, LEONARD	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment submitted on June 01, 04 and RCE filed 7/2/04. Claims 1-36 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazure et al (5,308,782) taken with Mukai (5,804,848) and Mukai Colinge (Article of "Reduction of Kink Effect...").

Mazure teaches (at Figs 1-14; col 3, line 1 through col 8) a method for forming a transistor on a substrate comprising at least the main steps of: forming a silicon on insulator (SOI) including an insulating layer on the substrate (col 3, lines 1-10); forming a first source/drain region 28 on the substrate (col 4, lines 26-55); vertically forming a body region on the first source/drain region, wherein vertically forming the body region 30 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 4 and 9; col 4, line 56 through col 5, line 44), wherein full channel region depletion is desired in order to achieve improved performance (col 14, lines 57-68); forming a second source/drain region 32/34 on the body region 30; forming a first gate 18/19 on a first one of the opposing sidewall surfaces with a first gate oxide 22 therebetween; forming a second gate 18 on a second oxide of the second one of the opposing sidewall surfaces with a second gate oxide 22 therebetween (Figs 4 and 9-10), wherein forming first source/drain region by ion implantation or epitaxial growing (col 4, lines 36-55). Re claims 31-36, wherein by forming a silicon on insulator (SOI), an insulating layer is formed between the body region and on the substrate (col 3, lines 1-10).

Mazure lacks mentioning the first gate formed with contact to couple to a first voltage source, and a second gate formed with a contact to couple to a second voltage source; and lacks mentioning thickness of the body region as a fully depleted structure with thin width relative to a doping concentration such that a bulk charge is negligible in transistor operation.

However, Colinge teaches to form a thin film transistor comprising a thin body channel region as fully depleted structure (page 97, left column; page 99), wherein the body region a

doping concentration (NA) and having a thin width thickness of about 100 nm that is sufficiently thin relative to the doping concentration such that a bulk charge (QB) has negligible effect in transistor operation, inherently. Mukai teaches (at Figure) forming a plurality of gate electrode including a first gate on a first one of the opposing sidewall surfaces, and a second gate on a second one of the opposing sidewall surfaces (Fig 15; col 1, lines 15-42; and Figs 1A,2-4, col 3-4), wherein the gate electrodes (23a-23d, 15a,15b) are independently of each other and applying a bias to the channel region in the body region 21 on one side of the gate electrodes (col 1, lines 37-42; col 2, lines 1-4; col 1, line 10-14; col 4, lines 7-18), that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure having from one to N conductive gate electrodes by operating the gate electrodes independently of each other and applying a bias to the channel region on one side of the gate electrodes, that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively, as taught by Mukai. This is because of the desirability to independently operate the gate electrodes independently each from the other, wherein the bulk charge (QB) can have a negligible effect in transistor operation due to low doping concentration and a thin width of the body region. Also it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure to have a thin thickness as taught by Colinge so as to form the thin film transistor comprising a thin body channel region operated as fully depleted structure. This is because of the desirability to reduce kink effect, current overshoots, and to form a very thin transistor. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure to have a thin thickness as taught by Colinge so as to form the thin film transistor comprising a thin body channel region operated as fully depleted structure. This is because of the desirability to reduce kink effect, current overshoots, and to form a very thin transistor. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of

thickness, as taught by the references including Mazure and Colinge, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233; In re Waite 77 USPQ 586 (CCPA 1948); In Re Swanson 56 USPQ 372 (CCPA 1942).

2. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,060,746) taken with Mukai (5,804,848) and Lidow et al (4,680,853).

Bertin et al teach a method (Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate comprising at least the main steps of: forming a first source/drain region on the substrate; vertically forming a body region 19 on the first source/drain region 23,12 (Figs 6,7) as a fully depleted structure (col 2, lines 17-21), wherein the body region has a low doping concentration (NA) and a thin width thickness of about 100 nm that is sufficiently thin relative to the low doping concentration such that a bulk charge (QB) has negligible effect in transistor operation, inherently, wherein vertically forming the body region 19 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 6,7; col 4, line 65 through col 5); forming a second source/drain region 22 on the body region; forming a first gate 15 on a first one of the opposing sidewall surfaces with a first gate oxide 18 therebetween (col 6); forming a second gate 15 on a second oxide 18 of the second one of the opposing sidewall surfaces with a second gate oxide therebetween, wherein forming first source/drain region by ion implantation, epitaxial growing or combination thereof (col 3, lines 40-47), wherein the body channel region having a thickness of 0.18 micron (col 2, lines 43-60), wherein the body region is encased with a ASG film and then annealing to diffuse the N-type dopant (col 5, lines 20-67), wherein CVD depositing and employing a BSG film as well known in the art for providing P-type dopant would have been obvious to one of ordinary skill in the art.

Berlin lacks mentioning the first gate formed with contact to couple to a first voltage source, and a second gate formed with a contact to couple to a second voltage source.

However, Mukai teaches (at Figure) forming a plurality of gate electrode including a first gate on a first one of the opposing sidewall surfaces, and a second gate on a second one of the opposing sidewall surfaces (Fig 15; col 1, lines 15-42; and Figs 1A,2-4, col 3-4), wherein the gate electrodes (23a-23d, 15a,15b) are independently of each other and applying a bias to the

channel region in the body region 21 on one side of the gate electrodes (col 1, lines 37-42; col 2, lines 1-4; col 1, line 10-14; col 4, lines 7-18), that is coupling the first and second the gate electrodes to a first voltage source and second voltage source through a contact, respectively, and there is a case of applying an equal voltage to each of the gate electrodes 23a-23d (col 5, lines 35-38, lines 28-38; col 4, lines 7-18). Lidow teaches (at Figure 2; col 6, lines 42-53) forming a plurality of contacts to the common gate, wherein contacts of the gate are coupled to first and second voltage sources of the same.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure having from one to N conductive gate electrodes by operating the gate electrodes independently of each other and applying a bias to the channel region on one side of the gate electrodes or applying an equal voltage to each of the gate electrodes, that is coupling the first and second the gate electrodes to a first voltage source and second voltage source of the same through a plurality of contacts, respectively, as taught by Mukai and Lidow. This is because of the desirability to supply a voltage source to the gate electrode, wherein, as in Lidow, R-C delay constant of the device is reduced by forming a plurality of contacts to the gate and coupling the first voltage source and second voltage source of the same.

3. Claims 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,060,746) taken with Mukai (5,804,848) and Lidow et al (4,680,853), as applied to claims 1-30 and further of Mazure et al (5,308,782),

Bertin et al teach a method (at Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate as applied to claims 1-30 above.

The references including Berlin lack forming an insulating layer on the substrate,

However, Mazure teaches (at col 3, lines 1-10) forming a transistor on a substrate, wherein the substrate includes a bulk silicon substrate or a silicon on insulator (SOI) substrate including a silicon layer on an insulating layer on a silicon substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Berlin on a silicon on insulator (SOI) substrate including an insulating layer on a silicon substrate as taught by Mazure, because these alternative

substrates are art recognized alternative for substitution, wherein substrate capacitance is reduced due to the insulating layer formed on the silicon substrate.

Response to Amendment

*** The terminal disclaimer filed on June 01, 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent Number 6,320,222 has been reviewed and is accepted. The terminal disclaimer has been recorded.

*** Applicant's remarks filed June 01, 2004 have been considered, but they are not persuasive and to be moot in view of the new ground(s) of rejection.

First, note that claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Herein, the limitations of "width is sufficiently thin relative to a doping concentration" and "negligible" are merely relative terms. Although the "bulk charge" is negligible in operation, the bulk charge still has a value by mathematic calculation.

Second, the relied references teaches forming a transistor having a fully depleted structure, wherein the body region has a low doping concentration (NA), wherein the body region has a very thin width (e.g. 100 nm in Bertin), which width is sufficiently thin relative to the low doping concentration so that a bulk charge (QB) can have negligible effect in transistor operation, inherently.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-7

Michael Trinh
Primary Examiner